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Silicon nano-transistors for logic applications

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Abstract

Silicon transistors have undergone rapid miniaturization in the past several decades. Recently reported CMOS devices have dimensional scales approaching the "nano-transistor" regime. This paper discusses performance characteristics of a MOSFET device with 15 nm physical gate length. In addition, aspects of a non-planar CMOS technology that bridges the gap between traditional CMOS and the nano-technology era will be presented. It is likely that this non-planar device will form the basic device architecture for future generations of nano-technology.
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1. Introduction

In order to improve performance and density, the size of Si MOS transistor has been scaled aggressively for the past 10 years. Fig. 1 shows the logic technology node and the corresponding transistor physical gate length (L_G) versus year of introduction [1]. It can be seen that the physical L_G has been scaled by more than 30% every 2 years. The Si MOS transistors that are currently in production have physical L_G of about 70 nm. The physical L_G is expected to decrease and will reach about 15 nm before 2009, and less than 10 nm early next decade. Research silicon transistors with physical L_G of 20 and 15 nm have already been demonstrated in our laboratory [2,3]. Considering that an influenza virus is only 100 nm, the size of silicon transistors produced today in factories and research

laboratories are already much smaller than a common virus. Thus the size of silicon transistors produced today is already in the "nano-regime" and can be termed "silicon nano-transistors". In this paper, we will show an example of a silicon nano-transistor with 15 nm L_G, discuss the fundamental scaling issues and potential solutions, and talk about a new transistor architecture that will become useful later this decade that can easily be considered to be a true bridging technology between conventional CMOS and the beginning of integrated silicon nano-transistors.

2. Silicon nano-transistors and scaling issues

Fig. 2 shows the TEM cross-section of a silicon nano-transistor with 15 nm physical L_G. The height of the polysilicon gate electrode for this device is 25 nm. The gate oxide used was nitrided SiO_2 with physical thickness of only 0.8 nm [4]. Figs. 3 and 4 show the

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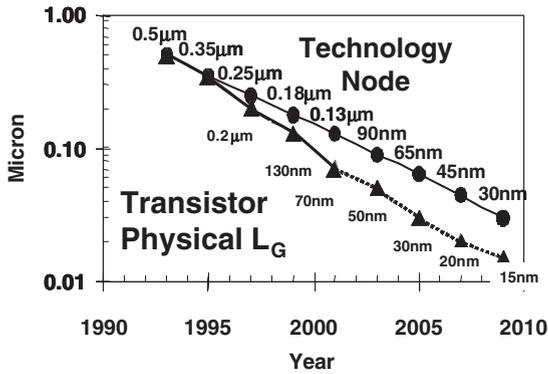 *E-mail address:* robert.s.chau@intel.com (R. Chau).

Fig. 1. Technology node and transistor physical L_G versus year.

Fig. 3. Family $I–V$ characteristics of the 15 nm MOS transistor.

Fig. 2. TEM cross-section of a 15 nm MOS transistor.
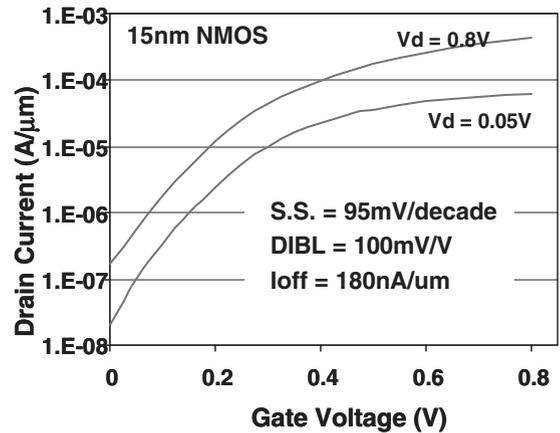
Fig. 4. Subthreshold $I–V$ characteristics of 15 nm MOS transistor.
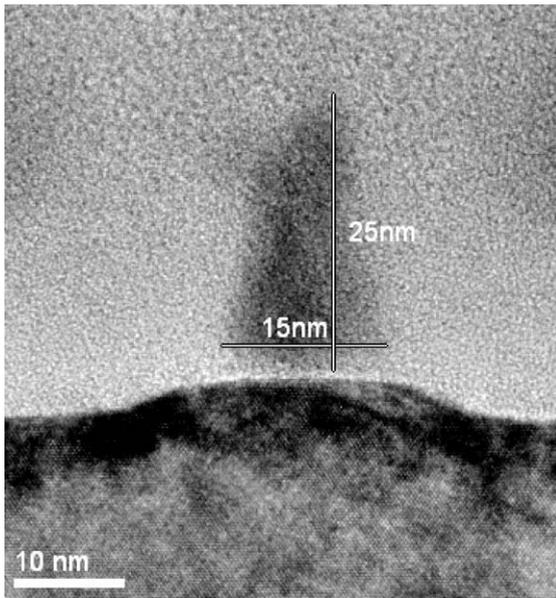
electrical characteristics of this device. It shows very reasonable short channel characteristics with subthreshold slope of 95 mV/decade and drain-induced barrier lowering (DIBL) of 100 mV/V. At supply voltage of 0.8 V, the transistor has drive current of 0.45 mA/μm and off-state leakage of 180 nA/μm. Continued improvement in device performance will require further gate oxide scaling, which will require the use of an alternative gate dielectric stack [5], since SiO_2 scaling is approaching its limit due to
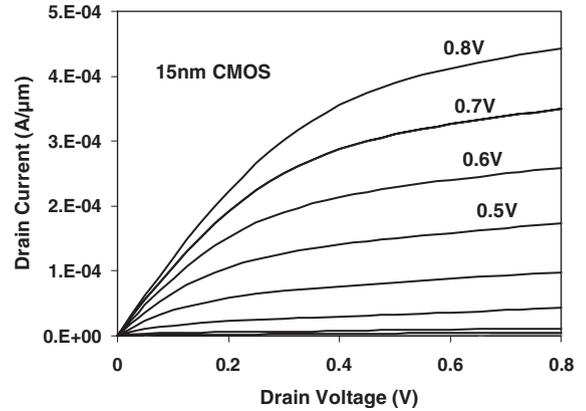
the increasing gate leakage with oxide scaling and the already-thin physical thickness. Another potential scaling issue is the continual increase in transistor off-state leakage with reducing physical L_G, as shown in Fig. 5 [1]. In order to control the power dissipation in future logic products, the trends of increasing off-state leakage and gate dielectric leakage need to be slowed down. One potential solution is to use a fully depleted silicon substrate to improve the short-channel performance such as the subthreshold slope and DIBL [6,7] which would allow for lower off-state leakage without impacting drive current in an adverse way. Fully depleted substrates can pose manufacturing challenges for high-volume manufacturing due to
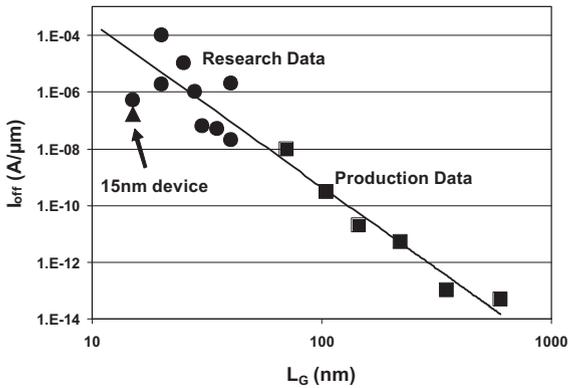
Fig. 5. Transistor off-state leakage (I_{off}) versus transistor physical L_{G}.
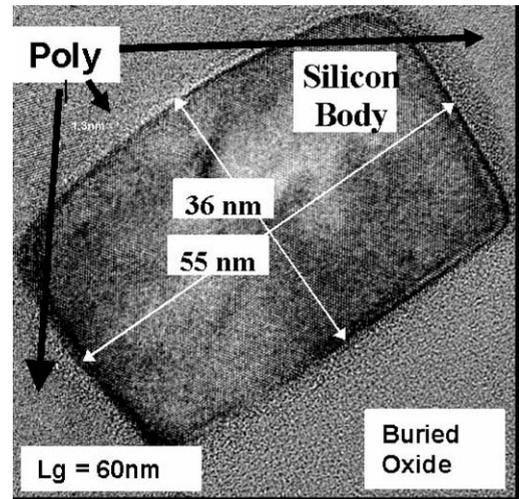

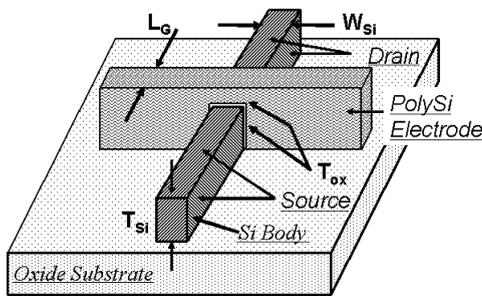Fig. 7. TEM cross-section of the experimental device.

Fig. 6. Schematic of a Tri-gate transistor.

the requirements of ultra-thin body thickness control needed for control of the electrical characteristics.

3. New transistor architecture for the nano-scale era

A new transistor architecture that can significantly improve the short-channel performance is the Tri-gate fully depleted silicon substrate transistor, as shown in Fig. 6 [7]. This transistor, normally fabricated on an oxide substrate, has a gate electrode on the top and two gate electrodes on the sides of the silicon body. The top-gate transistor has physical gate length L_{G} and physical gate width W_{Si}, while the side-gate transistor has physical gate length L_{G} and physical gate width T_{Si}, shown in Fig. 6. In general, Tri-gate transistors will typically have optimal performance

when $L_{G} = W_{Si} = T_{Si}$. In contrast to double-gate non-planar FINFET devices [8] where $W_{si} \sim \frac{2}{3} L_{G}$ or single-gate fully depleted DST [6] devices where $T_{si} \sim \frac{1}{3} L_{G}$ for purposes of controlling short-channel effects, the Tri-gate transistor has the least stringent silicon body thickness and width requirement and is the easiest to fabricate [7]. L_{G} is already the most stringent lithographic layer in modern CMOS circuits and allowing the Tri-gate to operate effectively when $L_{G} = W_{Si} = T_{Si}$, instead of sub-L_{G} design features is a tremendous advantage. A cross-section of an experimental $L_{G} = 60$ nm device is shown in Fig. 7 with $T_{Si} = 36$ nm and $W_{Si} = 55$ nm. The physical SiO_2 thickness is approximately 1.5 nm measured on the top of the device. The polysilicon gate runs along the vertical sidewalls and the top of the device. Fig. 8 shows the $I–V$ characteristics of the NMOS and PMOS transistors in a Tri-gate CMOS with physical $L_{G} = 60$ nm. Both transistors have excellent short channel performance with DIBL measured at 41 and 48 mV/V for the NMOS and PMOS devices, respectively. Likewise, the subthreshold slope is excellent with values of 68 mV/decade for the NMOS and 69.5 mV/decade for PMOS. These low values of the subthreshold slope and the absence of a kink demonstrate that the devices are fully depleted. The performance of the NMOS device was measured at $I_{Dsat} = 1.14$ mA/μm at an $I_{off} = 70$ nA/μm (measured at $V_{DS} = 1.3$ V).
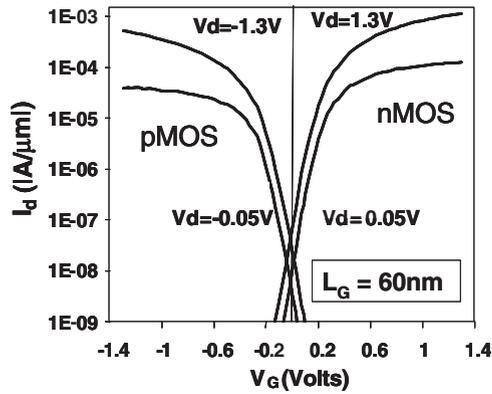
Fig. 8. Subthreshold I–V characteristics of the 60 nm Tri-gate CMOS.

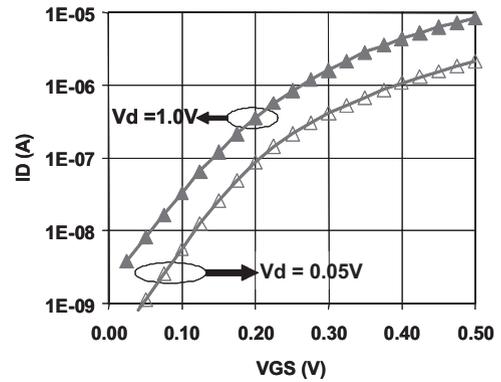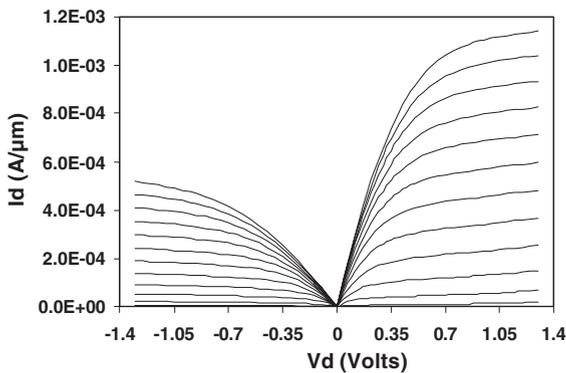Fig. 10. Simulated I–V characteristics of a 30 nm Tri-gate NMOS transistor.

Fig. 9. Family of curves for the 60 nm Tri-gate CMOS.

Fig. 11. SEM of the Tri-gate transistor showing multiple Si legs.

The PMOS I_{Dsat} was measured at 521 $\mu A/\mu m$ at $I_{off} = 24$ nA/ μm. In both cases, the normalization per unit width was measured from the TEM cross-section of the actual experimental device (shown in Fig. 6) and calculated as $Z = 2T_{Si} + W_{Si} = 2 \times 36 + 55 = 127$ nm. Fig. 9 illustrates the family of curves for these NMOS and PMOS devices. In order to better understand Tri-gate device performance as the devices are scaled, numerical simulations were performed on a device with $L_G = W_{Si} = T_{Si} = 30$ nm. Fig. 10 shows the simulated I–V characteristics of a Tri-gate silicon NMOS transistor with physical $L_G = W_{si} = T_{si} = 30$ nm done using a three-dimensional numerical device simulator. The 30 nm device has excellent short-channel performance with simulated subthreshold slope of 63 mV/decade (near ideal) and DIBL of 70 mV/V.
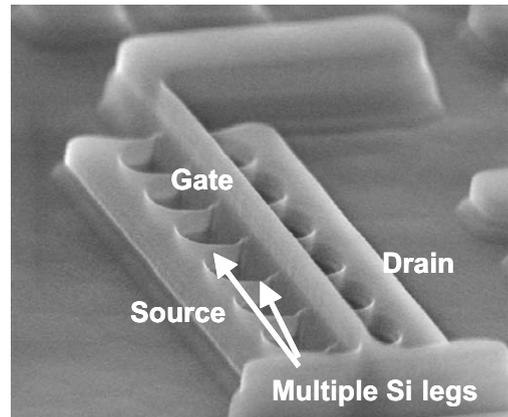
In order to increase the total drive current per unit design area, the Tri-gate transistors can be connected in parallel with a common gate electrode as illustrated in the SEM image reproduced in Fig. 11. The more silicon legs in a given design area, the higher the total drive current will be. Basic scaling shows that the total device current will be current per leg multiplied by the total number of legs. The resulting top-view of the final layout will look like Fig. 12 which compares both standard planar layout with the modified Tri-gate layout approach. In the future, the silicon legs can scale to form Si nano-wires [9], be replaced by devices such as carbon nano-tubes [10], or accommodate non-Si quantum wire structures.
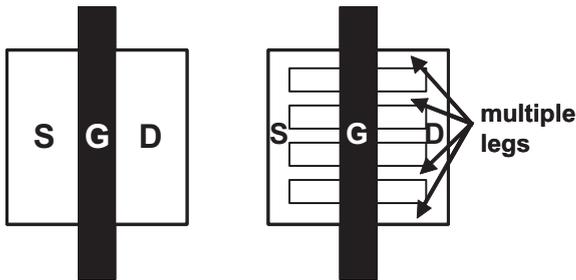
Fig. 12. Top view of transistor layout comparing the planar (left) and the Tri-gate layout (right) showing multiple Tri-gate legs.

4. Summary

Based on projections, transistor physical L_G will reach about 15 nm before end of this decade. Research silicon nano-transistors with 15 nm physical L_G have already been demonstrated with reasonable switching characteristics. Two scaling issues, namely increases in gate and transistor off-state leakage, will need to be solved in order to control power dissipation in future logic products. The former will require an alternative gate stack to solve, and the latter will require a new transistor architecture such as the Tri-gate fully depleted-substrate transistor to solve. In the future, the Tri-gate transistor architecture will be compatible with new electronic devices such as silicon nano-wires, carbon nano-tubes, or non-Si quantum wire structures.

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